A novel ring-based triple-push voltage-controlled oscillator (VCO) with a continuous range from 0.2 to 34 GHz is proposed and realized using a commercial 0.13-μm 1P8M CMOS VCO process. The output power of the VCO is -18 dBm and there is with a ±2 dB variation in the full band. The fundamental rejection is more than 15 dB and the second harmonic rejection is more than 25 dB. This VCO achieves the widest continuously tuning range reported to date.

The local oscillator is a key component in wide band and high-speed applications. Due to the ever increasing demand for bandwidth, the tuning range of the voltage-controlled oscillator (VCO) is an important feature in the production of microwave and millimeter-wave frequencies. Most LC VCOs are usually used for narrow band design due to fixed inductors [1], [2], [4]. There are several approaches to enhance the tuning range, which include the use of such as switch capacitor, a duplicate oscillator or frequency mixing [3]. Most of these approaches consume large chip size and complex design in system. Ring oscillators can easily achieve a wide tuning range with a small chip size, but they suffer from the oscillation frequency limitations and high power dissipation at high frequency. For example, the highest fundamental ring oscillator in a SiGe HBT with $f_T$ of 120 GHz is proposed at 32 GHz in [5].

In stead of adopting high $f_{max}$ process technology, there are circuit...
structures that could be used instead of adopting high \( f_{max} \) process technology, to increase the tuning range as well as to achieve higher oscillation frequencies. The multi-push VCO is an attractive choice because it cancels the fundamental signals and sums up the desired in-phase multiple harmonics as the output signal. In traditional topologies, it is usually composed of several identical oscillators. However, the multi-push VCO, but it has the problem of disadvantage of large chip size and process variation [6].

A new topology is proposed to overcome the frequency limitation of a ring oscillator, a new topology is proposed. Fig. 1 shows the block diagram of a multi(M)-push topology with an \( N \)-stage ring oscillator. Where, \( M \) could be a factor of \( N \). The oscillation frequency of a ring oscillator can be derived using the multi-push \( M \), the current \( I_{ctrl} \), the number of stages \( N \), the amplitude \( V_{osc} \) and the parasitic capacitance \( C_{G} \). In Fig.1, large number of stage brings up low frequency. To decrease the effect in frequency from number of stage, the value of \( M \) can be selected equal to \( N \). This enhances the oscillation frequency of different stages is enhanced and brings them closer to each other. Due to the large power consumption and complex layout routing of more number of stages is not recommended since it would result in large power consumption and complex layout routing suggested. Furthermore, the value of \( M \) and \( N \) equals to three shows the highest frequency is seen when the values of both \( M \) and \( N \) are equal to three (Fig. 1). The use of the triple-push topology VCO that combines the three-stage ring oscillator and the triple-push topology is proposed in a commercial 0.13- \( \mu \)m 1P8M CMOS process. The triple-push approach enhances the oscillation frequency and the tuning range of a ring oscillator. It also greatly reduces the power dissipated in a ring oscillator at high frequency. An appropriate

\[ \text{Comment [a9]: CHECK: Is this a known technical term? IF not, you may want to change it to make the meaning clearer.} \]

\[ \text{Comment [a10]: TUTOR: This sentence is well written and well structured.} \]

\[ \text{Comment [a11]: CHECK: Is the term commonly written as 'multi-push' or 'multi push'? Please use the term the same way throughout the document.} \]

\[ \text{Comment [a12]: CHECK: You may want to clarify what is meant by 'process variation' here.} \]

\[ \text{Comment [a13]: TUTOR – Grammar: Incorrect: a N-stage} \]

\[ \text{Correct: an N-stage} \]

\[ \text{Reason: When pronouncing ‘N’ the sound starts with a vowel (read: en). Therefore, use ‘an’.} \]

\[ \text{Example: A T-stage…} \]

\[ \text{Example: An N-stage…} \]

\[ \text{Example: An M-stage…} \]

\[ \text{Comment [a14]: CHECK: The meaning of this sentence is unclear, please rephrase.} \]

\[ \text{Comment [a15]: CHECK: The meaning of this sentence is unclear, please rephrase.} \]

\[ \text{Comment [a16]: CHECK: Is enhances the word you would like to use here? Perhaps 'increases' would be more appropriate?} \]

\[ \text{Comment [a17]: CHECK: Is this the correct interpretation of the meaning of this sentence?} \]

\[ \text{Comment [a18]: TUTOR - Word choice: OK: ‘saves power’} \]

\[ \text{Better: ‘reduces the power dissipated’} \]

\[ \text{Reason: It is better to say that the power is ‘reduced’ rather than ‘saved’ in this context since only the power usage in the experiment is relevant to the reader.} \]

\[ \text{Comment [a19]: TUTOR - Word Choice: The use of words like ‘greatly’ should be avoided when no specific value is given. e.g. Here ‘greatly’ conveyed no meaning since it did not convey any additional information... [1]} \]
topology for the triple push approach is an appropriate topology for the triple-push approach. Since there is only the odd mode in three-stage ring oscillator, the fundamental and second harmonics will cancel out. In addition, a three-stage ring oscillator since it can naturally provide three signals with a 120° phase shift is an appropriate topology for the triple-push approach. Since there is only the odd mode in three-stage ring oscillator, the fundamental and second harmonics will cancel out. In addition, a three-stage ring oscillator since it can naturally provide three signals with a 120° phase shift is an appropriate topology for the triple-push approach. Since there is only the odd mode in three-stage ring oscillator, the fundamental and second harmonics will cancel out.

The circuit schematic is shown in Fig. 2. A conventional ring oscillator with a PMOS as resistive load and current control and is used as well as a 16-finger NMOS with a total gate width of 32 μm are used. The circuit also uses a 12-finger PMOS with a total gate width of 120 μm which ensures that the small voltage drop between the drain and the source is small. The NMOS device trade off between the parasitic capacitance and the transconductance to reach the highest frequency. The PMOS device is chosen to have a selected large gate width to lower the voltage drop in \( V_{DS} \). However, the large gate width causes results in a decrease in the oscillation frequency.

In the tuning mechanism, the gate bias of the PMOS is selected so that it controlled to turns on the current through the NMOS. The breakdown voltage between the gate and the source in the PMOS determines the lower limit of the control voltage is limited by the breakdown voltage between the gate and the source in the PMOS, where the PMOS provide the highest current, and the PMOS is in the triode region. The PMOS offers low resistance, which reduces the RC delay. The upper limit of the control voltage is the current level that satisfies the oscillation condition, which is the worst case, where the PMOS is in the saturation region and offers low resistance to low frequency oscillation in low frequency. In order to make the oscillation frequency as high as possible, all the parasitic capacitances in the loop should be reduced to make the oscillation frequency as high as possible. The current source is removed to decrease the noise source and enhance the voltage headroom. Since the larger current generates...
larger higher output power at a high frequency, the output power increases with the frequency. As the power gain degrades at high frequency, the common source buffer is used to flatten the curve of the output power versus the tuning frequency due to the degradation of power gain at high frequency. This and thus prevents the loading effect from the transmission lines due to power combination. The size of the buffer, a 12-finger NMOS with 24-μm gate width, is a trade off between the parasitic capacitance and the flatness of output power. In order to enhance the fundamental and the second harmonic rejection, any asymmetry in the loop in terms of phase errors or process variation should be minimized to enhance the fundamental and the second harmonic rejection. A thin-film microstrip (TFMS) line is used to combine the three signals after the drain of buffers. Each drain of the PMOS is connected to the VDD with an equal length of TFMS. The gates are biased using through 5 kΩ resistors. The control voltage and VDD are naturally virtually short by nature.

Measurements on this CMOS VCO are carried out by on-wafer probing. Measurements on the output port are done through bias-T. Fig. 3 shows the measured current and control voltage versus the oscillation frequency. The output frequency can be continuously tuned in the range from 0.2 GHz to 34 GHz with the control voltage varying between 1.75 V and 0.85 V, and with the core current varying from 0.5 mA to 35 mA. The VDD is 2 V, and the buffer is 0.7 V with 7 mA. The output power is -18 dBm with ±2dB variation, as is shown in Fig. 4. The measured fundamental rejection is more than 15 dB and the second harmonic rejection is more than 25 dB. The phase noise for a 1 -MHz offset frequency ranges from -75.6 dBC/Hz to -69.2 dBC/Hz and for a 10-MHz offset frequency, it ranges from -98.3 to -92.6 dBC/Hz. The phase noise has a degradation by an amount of 9.54 dBC compared to the fundamental phase noise.
due to the triple-push mechanism. Fig. 5 shows the chip photo of the triple-push VCO. It has a compact chip size of 0.34 x 0.28 mm², which includes the area of the pads. The core area is only 0.19 x 0.13 mm². Fig. 6 lists the performance of recently wide-band Si-based VCOs. The work that this paper talks about achieves the widest tuning range and smallest chip size.

A ring-based triple-push VCO that has been proposed was proposed. Using the triple-push topology, the tuning range is tripled in the triple-push topology with a good linearity. Due to the absence of inductors, a very small chip size, including the bonding pad is achieved. To the best of the author’s knowledge, this VCO offers the widest continuous tuning range and the smallest chip size among all of the VCOs reported to date. It demonstrates the potential for applications in the microwave to millimeter wave regime in CMOS technology.

References:


Figure 1: Ring-based multi-push topology and simulated oscillation frequency comparison of multi-stage.

Comment [a43]: CHECK: It may be better to separate these images and use different captions to avoid confusing the reader. You could label the images using a, b, c etc.
Figure 2: Schematic of the ring-based triple-push VCO.
Figure 3: Tuning Characteristics.
Figure 4: Measurement results.
Figure 5: Chip photo of the triple-push VCO with a chip size of 0.34 x 0.28 mm²

\[ 3f_0 \]

\[ V_{DD} \]

\[ V_{ctrl} \]

0.34 mm
<table>
<thead>
<tr>
<th>Oscillation Frequency / Process</th>
<th>Phase noise (dBc/Hz)</th>
<th>Core DC power (mW)</th>
<th>Tuning range (GHz) and Percentage(%)</th>
<th>Frequency Ratio ($F_{\text{max}}/F_{\text{min}}$)</th>
<th>Chip Area (mm²)</th>
<th>Reference</th>
</tr>
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<tr>
<td>34 GHz 0.13-μm CMOS</td>
<td>-98.3</td>
<td>2-70</td>
<td>0.2-34 (197.6 %)</td>
<td>170</td>
<td>0.095</td>
<td>This Work</td>
</tr>
<tr>
<td>7 GHz 65-nm CMOS</td>
<td>-110 dBc</td>
<td>7.2-42</td>
<td>3.2-7.3 (78 %)</td>
<td>2.3</td>
<td>0.2 (Active area)</td>
<td>[1]</td>
</tr>
<tr>
<td>29.4 GHz 0.13-μm CMOS</td>
<td>-96.2 dBc</td>
<td>36.5</td>
<td>23.2-29.4 (23.6%)</td>
<td>1.26</td>
<td>1.4</td>
<td>[2]</td>
</tr>
<tr>
<td>23 GHz 0.25-μm SiGe BiCMOS</td>
<td>-101.2 dBc</td>
<td>9</td>
<td>18.23 (24.3 %)</td>
<td>1.28</td>
<td>--</td>
<td>[4]</td>
</tr>
<tr>
<td>32 GHz $f_c$/120 GHz SiGe HBT</td>
<td>-85.3 dBc</td>
<td>87</td>
<td>28.52 (13.3%)</td>
<td>1.14</td>
<td>0.28</td>
<td>[5]</td>
</tr>
</tbody>
</table>

Figure 6: Summary of measured performance and comparison with recently reported wide-band VCOs.
TUTOR - Word Choice:

The use of words like 'greatly' should be avoided when no specific value is given. E.g. Here 'greatly' conveyed no meaning since it did not convey any additional information to the reader.